LOW RESISTANCE INTEGRATED CIRCUIT MOS TRANSISTOR

ABSTRACT OF THE INVENTION

A gate structure (30) is formed on a semiconductor (10). Source and drain extension regions (130) are formed in the semiconductor (10) adjacent to the gate structure (30). Metal silicide layers (140) are formed on the extension regions (130) and sidewall structures (155, 165, and 175) are formed over the metal silicide layers (140). Source and drain regions (120) are formed in the semiconductor (10), and metal silicide layers (180) are formed on the source and drain regions (120).